

CLAIMS

1. A semiconductor apparatus includes a substrate with a pad, an internal circuitry region, 5 and a protection resistance formed on the substrate, the semiconductor apparatus comprising:

the pad being connected to a first electrode of the protection resistance by a wiring;

the internal circuitry region being 10 connected to a second electrode of the protection resistance by a wiring; and

the protection resistance protecting the internal circuitry region from electrostatic discharging;

15 wherein the pad is placed between the protection resistance and the internal circuitry region.

2. The semiconductor apparatus as claimed 20 in claim 1, wherein a distance between the pad and the first electrode and a distance between the pad and the second electrode are substantially the same.

3. A semiconductor apparatus includes a substrate with a pad, an internal circuitry region, and a protection resistance formed on the substrate, the semiconductor apparatus comprising:

5 the pad being connected to a first electrode of the protection resistance by a wiring;

the internal circuitry region being connected to a second electrode of the protection resistance by a wiring; and

10 the protection resistance protecting the internal circuitry region from electrostatic discharging;

wherein a distance between the first electrode and the internal circuitry region is greater than a distance between the second electrode and the internal circuitry region.

4. The semiconductor apparatus as claimed in claim 3, wherein the substrate is provided with a 20 guard ring region surrounding the pad, the internal circuitry region, and the protection resistance; and distances from two sides of the first electrode being rectangular to the guard ring region adjacent to the first electrode are substantially 25 equal.

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5. The semiconductor apparatus as claimed
in claim 4, wherein the protection resistance
comprises a well region formed in the substrate; and
distances from the two sides of the first
5 electrode to edge portions of the well region
adjacent to the first electrode are substantially
equal.

6. The semiconductor apparatus as claimed
10 in claim 5, wherein distances from two edge portions
of the well region to the guard ring region adjacent
to the well region are substantially equal.

7. The semiconductor apparatus as claimed
15 in claim 3, wherein the pad is placed on an
insulating layer on the protection resistance.

8. The semiconductor apparatus as claimed
in claim 1, wherein the protection resistance is
20 formed by an impurity diffusion layer.

9. The semiconductor apparatus as claimed
in claim 1, wherein a protection circuit is formed
by the protection resistance and a protection
25 transistor included in the internal circuitry region.